

WHAT IS CLAIMED IS:

- 1 1. A circuit comprising:
2 first and second field effect transistor devices arranged
3 to provide parallel current paths between a supply voltage and
4 an output node, the first and second transistor devices having
5 oxide layers with a thickness of about 200 Angstroms or less;
6 and
7 a component coupled to the output node that is intolerant
8 of the supply voltage.
- 1 2. The circuit of claim 1 wherein the oxide layers have a
2 thickness between about 100 Angstroms and about 190 Angstroms.
- 1 3. The circuit of claim 1 further comprising a current source
2 coupled to the output node.
- 1 4. The circuit of claim 1 further comprising a third
2 transistor device coupled to the output node and a circuit
3 that activates the third transistor device when the first
4 transistor device is deactivated.
- 1 5. The circuit of claim 1 further comprising switching logic
2 to selectively activate the first transistor device.

1 6. The circuit of claim 1, wherein the transistor devices are
2 selected from the group consisting of P devices and S devices.

1 7. The circuit of claim 6, wherein the first transistor
2 device is a P device and the second transistor device is an S
3 device.

1 8. The circuit of claim 7, wherein the S device is diode-
2 connected to the voltage source.

1 9. The circuit of claim 1, wherein a third transistor device
2 is disposed between the first transistor device and the output
3 node and wherein the third transistor device has an oxide
4 layer with a thickness greater than about 200 Angstroms.

1 10. The circuit of claim 1, wherein the supply voltage is
2 selected from the group consisting of about 3 volts, about 5
3 volts and about 12 volts.

1 11. A computer system, comprising:
2 a central processor;
3 a system bus coupled to the processor;
4 a main memory coupled to said system bus; and
5 a programmable non-volatile long term memory coupled to
6 said system bus, further comprising:

7 a flash EEPROM memory array; and
8 a circuit for providing a voltage substantially
9 higher than Vcc to the EEPROM array, said circuit
10 comprising:

11 first and second field effect transistor
12 devices arranged to provide parallel current paths
13 between a supply voltage and an output node, the
14 first and second transistor devices having oxide
15 layers with a thickness of about 200 Angstroms or
16 less; and

17 a component coupled to the output node that is
18 intolerant of the supply voltage.

1 12. The system of claim 11 wherein the oxide layers have a
2 thickness of about 100 to about 190 Angstroms.

1 13. The system of claim 11 further comprising a current
2 source coupled to the output node.

1 14. The system of claim 11 further comprising a third
2 transistor device coupled to the output node and pull down
3 switching logic that activates the transistor when the first
4 transistor device is deactivated.

1 15. The system of claim 11 further comprising switching logic
2 to selectively activate the first transistor device.

1 16. The system of claim 11, wherein the transistor devices
2 are selected from the group consisting of P devices and S
3 devices.

1 17. The system of claim 16, wherein the first transistor
2 device is a P device and the second transistor device is an S
3 device.

1 18. The system of claim 17, wherein the S device is diode-
2 connected to the voltage source.

1 19. The system of claim 11, wherein a third transistor device
2 is disposed between the first transistor device and the output
3 node and wherein the third transistor device has an oxide
4 layer with a thickness greater than about 200 Angstroms.

1 20. The system of claim 11, wherein the supply voltage is
2 selected from the group consisting of about 3 volts, about 5
3 volts and about 12 volts.

1 21. A method comprising:

2 providing first and second field effect transistor
3 devices arranged to provide parallel current paths between a
4 supply voltage and an output node, the first and second
5 transistor devices having oxide layers with a thickness of
6 about 200 Angstroms or less, wherein the output node is
7 coupled to a component that is intolerant of the supply
8 voltage; and

9 selectively activating the first transistor device to
10 pass substantially the entire supply to the output node.

1 22. The method of claim 21, further comprising bleeding sub-
2 threshold current from the output node.

1 23. The method of claim 22, wherein the bleeding is performed
2 by a current source coupled to the output node.

1 24. The method of claim 21, further comprising pulling down
2 the output node voltage to the steady state output node
3 voltage upon deactivation of the first transistor device.

1 25. The method of claim 24 wherein the pull down is effected
2 by a third transistor device coupled to the output node and
3 logic that activates the transistor when the first transistor
4 device is deactivated.

1 26. The method of claim 21 wherein the oxide layers have a
2 thickness of about 100 to about 190 Angstroms.

1 27. The method of claim 21 wherein the first transistor
2 device is activated by a logic network.

1 28. The method of claim 21, wherein the transistor devices
2 are selected from the group consisting of P devices and S
3 devices.

1 29. The method of claim 28, wherein the first transistor
2 device is a P device and the second transistor device is an S
3 device.

1 30. The method of claim 29, wherein the S device is diode-
2 connected to the voltage source.

1 31. The method of claim 21, wherein the supply voltage is
2 selected from the group consisting of about 3 volts, about 5
3 volts and about 12 volts.